REMARKS

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached pages are captioned "**Version with Markings to Show Changes Made**."

No new matter has been introduced by any of the above amendments. In light of the above amendments and remarks, Applicant believes that Claims 1-27 are in condition for allowance, and allowance of the application is therefore requested.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as **first class mail** in an envelope addressed to: Commissioner for Patents, Washington, D.C., 20231, on October 10, 2002.

Pat Slaback
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Signature

VERSION WITH MARKINGS TO SHOW CHANGES MADE

CLAIMS

14. (Amended) A system for flexibly accessing nested JTAG TAP controllers for IP cores in a FPGA-based SoC, the [method] system comprising:

a selector for choosing at least one IP core JTAG TAP controller from a plurality of JTAG TAP controllers nested in the FPGA-based SoC; and

a multiplexer for programmably connecting said at least one IP core JTAG TAP controller to a host JTAG TAP controller.

21. (New) A system for performing boundary scan functions on a plurality of IP cores, the system comprising:

an FPGA-based system-on-chip (SoC) comprising a plurality of IP cores each including a first JTAG TAP controller; and

a host JTAG TAP controller coupled to each of the first JTAG TAP controllers.

22. (New) The system of Claim 21, wherein the FPGA-based SoC includes the host JTAG TAP controller.

23. (New) The system of Claim 21, further comprising:

a selector circuit coupled between the first JTAG TAP controllers and the host JTAG TAP controller.

24. (New) The system of Claim 23, wherein the FPGA-based SoC includes the host JTAG TAP controller and the selector circuit.

25. (New) The system of Claim 21, wherein the host JTAG TAP controller comprises:

a selectable bit register having an input terminal coupled to the selector circuit and further having an output terminal providing a selected bit; and

an instruction register having an input terminal coupled to the output terminal of the selectable bit register, the instruction register having an output terminal providing an instruction having an apparently extended length.

26. (New) The system of Claim 25, further comprising:

a selector circuit coupled between the first JTAG TAP controllers and the host JTAG TAP controller.

27. (New) The system of Claim 25, wherein the FPGA-based SoC includes the host JTAG TAP controller.